NUS3046MN

Overvoltage Protection IC with Integrated MOSFET

This device represents a new level of safety and integration by combining the NCP346 overvoltage protection circuit (OVP) with a 30 V P−channel power MOSFET. This IC is specifically designed to protect sensitive electronic circuitry from overvoltage transients and power supply faults. During such hazardous events, the IC quickly disconnects the input supply from the load, thus protecting the load before any damage can occur.

The OVP IC is optimized for applications that use an external AC−DC adapter or a car accessory charger to power a portable product or recharge its internal batteries. It has a nominal overvoltage threshold of 5.5 V which makes it ideal for single cell Li−Ion as well as 3/4 cell NiCD/NiMH applications.

Features

- Overvoltage Turn−Off Time of Less Than 1.0 μs
- Accurate Voltage Threshold of 5.5 V, Nominal
- Control Input Compatible with 1.8 V Logic Levels
- −30 V Integrated P−Channel Power MOSFET
- Low $R_{DS(on)}$ = 66 mΩ @ −4.5 V
- Low Profile 3.3 x 3.3 mm DFN Package Suitable for Portable Applications
- Maximum Solder Reflow temperature @ 260°C
- This is a Pb−Free Device

Benefits

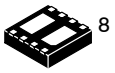
- Provide Battery Protection
- Integrated Solution Offers Cost and Space Savings
- Integrated Solution Improves System Reliability

Applications

- Portable Computers and PDAs
- Cell Phones and Handheld Products
- Digital Cameras

ON Semiconductor®

http://onsemi.com



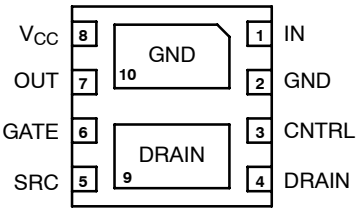
DFN8
CASE 506AL

MARKING DIAGRAM

3046	= Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



(Bottom View)

ORDERING INFORMATION

Device	Package	Shipping†
NUS3046MNT1G	DFN8 (Pb−Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

June, 2006 − Rev. 1

Publication Order Number:
NUS3046MN/D

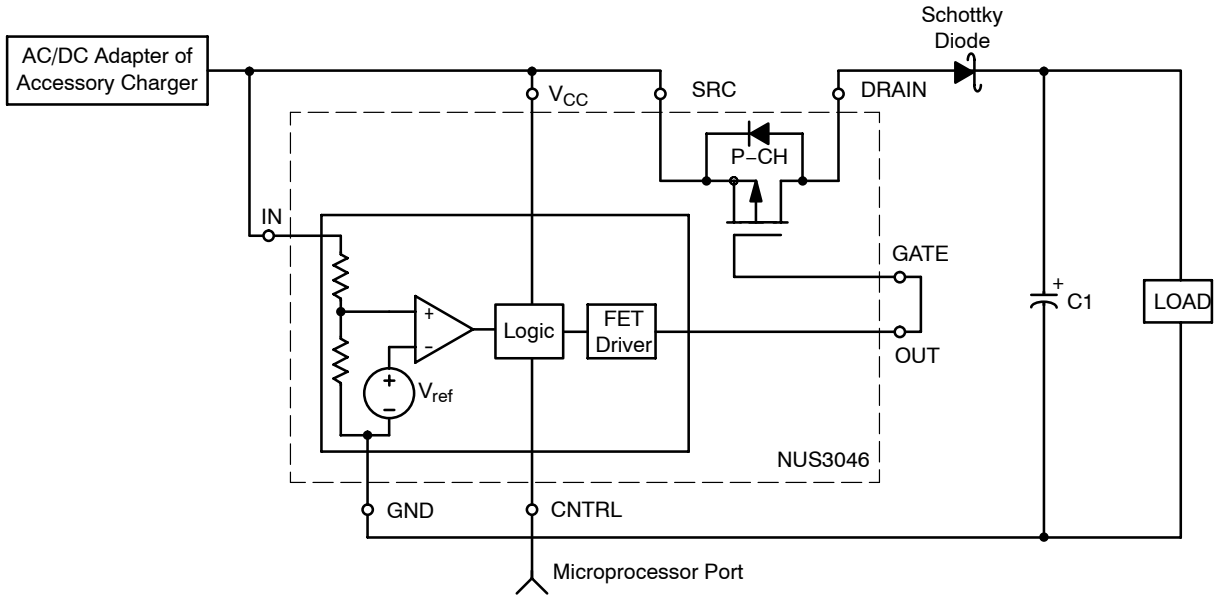


Figure 1. Simplified Schematic

PIN FUNCTION DESCRIPTIONS

Pin #	Symbol	Pin Description
1	IN	This pin senses an external voltage point. If the voltage on this input rises above the overvoltage threshold (V_{TH}), the OUT pin will be driven to within 1.0 V of V_{CC}, thus disconnecting the P−channel power MOSFET. The nominal threshold level is 5.5 V and this threshold level can be increased with the addition of an external resistor between IN and V_{CC}.
2, 10	GND	Circuit Ground
3	CNTRL	This logic signal is used to control the state of OUT and turn−on/off the P−channel power MOSFET. A logic High results in the OUT signal being driven to within 1.0 V of V_{CC} which disconnects the FET. If this pin is not used, the input should be connected to ground.
4, 9	DRAIN	Drain pin of the P−channel power MOSFET
5	SRC	Source pin of the P−channel power MOSFET
6	GATE	Gate pin of the P−channel power MOSFET
7	OUT	This signal drives the gate of a P−channel MOSFET. It is controlled by the voltage level on IN or the logic state of the CNTRL input. When an overvoltage event is detected, the OUT pin is driven to within 1.0 V of V_{CC} in less than 1.0 μsec provided that gate and stray capacitance is less than 12 nF.
8	V_{CC}	Positive Voltage supply. P−channel power MOSFET is guaranteed to be in ON state as long as V_{CC} remains above 2.5 V and below the overvoltage threshold.

OVERVOLTAGE PROTECTION CIRCUIT TRUTH TABLE

IN	CNTRL	OUT
$<V_{th}$	L	GND
$<V_{th}$	H	V_{CC}
$>V_{th}$	L	V_{CC}
$>V_{th}$	H	V_{CC}

MAXIMUM RATINGS (T_A = 25°C unless otherwise stated)

Rating	Pin	Symbol	Min	Max	Unit
OUT Voltage to GND	7	V_O	−0.3	30	V
Input and CNTRL Pin Voltage to GND	1 3	V_{input} V_{CNTRL}	−0.3 −0.3	30 13	V
V_{CC} Maximum Range	8	$V_{CC(max)}$	−0.3	30	V
Maximum Power Dissipation (Note 1)	−	P_D	−	1.0	W
Thermal Resistance Junction−to−Air (Note 1) OVP IC P−Channel FET	−	$R_{\theta JA}$	 − −	 108.6 104.3	°C/W
Junction Temperature	−	T_J	−	150	°C
Operating Ambient Temperature	−	T_A	−40	85	°C
V_{CNTRL} Operating Voltage	3	−	0	5.0	V
Storage Temperature Range	−	T_{stg}	−65	150	°C
ESD Performance (HBM) (Note 2)	1, 2, 3, 7, 8, 10	−	2.5	−	kV
Drain−to−Source Voltage		V_{DSS}		−30	V
Gate−to−Source Voltage		V_{GS}	−20	20	V
Continuous Drain Current, Steady State, T_A = 25°C (Note 1)		I_D		−1.0	A

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface−mounted on FR4 board using 1 inch sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Human body model (HBM): MIL STD 883C Method 3015−7, (R = 1500 Ω, C = 100 pF, F = 3 pulses delay 1 s).

OVERVOLTAGE PROTECTION IC ELECTRICAL CHARACTERISTICS (T_A= 25°C, V_{CC} = 6.0 V, unless otherwise specified)

Characteristic	Symbol	Pin	Min	Typ	Max	Unit
V_{CC} Operating Voltage Range	$V_{CC(opt)}$	8	$2.5^{(+3)}$	–	25	V
Supply Current (I_{CC} + I_{Input}; V_{CC} = 5.0 V Steady State)	I_{supply}	1, 8	–	0.75	1.2	mA
Input Threshold (V_{Input} connected to V_{CC}; V_{Input} increasing)	V_{Th}	1	5.3	5.5	5.7	V
Input Hysteresis (V_{Input} connected to V_{CC}; V_{Input} decreasing)	V_{Hyst}	1	20	50	200	mV
Input Impedance (Input = V_{Th})	R_{in}	1	30	60	100	kΩ
CNTRL Voltage High (V_{CC} = V_{in} = 4.0 V)	V_{ih}	3	1.5	–	–	V
CNTRL Voltage Low (V_{CC} = V_{in} = 4.0 V)	V_{il}	3	–	–	0.5	V
CNTRL Current High ($V_{ihCNTRL}$ = 5.0 V, V_{CC} = V_{in} = 5.0 V)	I_{ih}	3	–	95	200	μA
CNTRL Current Low ($V_{ilCNTRL}$ = 0.5 V, V_{CC} = V_{in} = 5.0 V)	I_{il}	3	–	10	20	μA
Output Sink Current (V_{CC} = V_{in} = 5.0 V; V_{OUT} = 1.0 V)	I_{Sink}	7	4	10	16	μA
Output Voltage High (V_{CC} = V_{in} = 5.0 V; CNTRL = 0 V, I_{Source} = 10 mA) Output Voltage High (V_{CC} = V_{in} = 5.0 V; CNTRL = 0 V, I_{Source} = 0.25 mA) Output Voltage High (V_{CC} = V_{in} = 5.0 V; CNTRL = 0 V, I_{Source} = 0 mA)	V_{oh}	7	V_{CC} – 1.0 V_{CC} – 0.25 V_{CC} – 0.1	–	–	V
Output Voltage Low (V_{CC} = V_{in} = 5.0 V; I_{Sink} = 0 mA; CNTRL = 0 V)	V_{ol}	7	–	–	0.1	V
Turn ON Delay – Input (Note 3) (V_{Input} connected to V_{CC}; V_{Input} step down signal from 6.0 to 5.0 V; measured to 50% point of OUT)	$T_{ON\ IN}$	7	–	1.8	–	ms
Turn OFF Delay – Input (V_{Input} connected to V_{CC}; CNTRL = 0 V; V_{Input} stepup signal from 5.0 to 6.0 V; C_L = 12 nF; Output > V_{CC} – 1.0 V)	$T_{OFF\ IN}$	7	–	0.5	1.0	μs
Turn ON Delay – CNTRL (V_{CC} = V_{in} = 5.0 V; CNTRL step down signal from 2.0 to 0.5 V; measured to 50% point of OUT) (Note 3)	$T_{ON\ CT}$	7	–	10	–	μs
Turn OFF Delay – CNTRL (V_{CC} = V_{in} = 5.0 V;CNTRL step up signal from 0.5 to 2.0 V; C_L = 12 nF; Output > V_{CC} –1.0 V)	$T_{OFF\ CT}$	7	–	0.6	1.0	μs

3. Guaranteed by design.

P–CHANNEL MOSFET ELECTRICAL CHARACTERISTICS (T_A= 25°C unless otherwise specified)

Parameter	Symbol	Min	Typ	Max	Units
Drain to Source On Resistance V_{GS} = –4.5 V, I_D = –600 mA V_{GS} = –4.5 V, I_D = –1.0 A	$R_{DS(on)}$		 66 66	 110 110	mΩ
Zero Gate Voltage Drain Current V_{GS} = 0 V, V_{DS} = –24 V	I_{DSS}			 –1.0	μA
Turn On Delay (Note 4) V_{GS} = –4.5 V, I_D = –1.0 A, R_G = 6.0 Ω, V_{DS} = –15 V	$t_{d(on)}$		11		ns
Turn Off Delay (Note 4) V_{GS} = –4.5 V, I_D = –1.0 A, R_G = 6.0 Ω, V_{DS} = –15 V	$t_{d(off)}$		28		ns
Input Capacitance (Note 3) V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = –15 V	C_{in}		750		pF
Gate to Source Leakage Current V_{GS} = ±20 V, V_{DS} = 0 V	I_{GSS}		±10		nA
Drain to Source Breakdown Voltage V_{GS} = 0 V, I_D = –250 μA	$V_{(BR)DSS}$	 30			V
Gate Threshold Voltage V_{GS} = V_{DS}, I_D = –250 μA	$V_{(GS)th}$	 –3.0		 –1.0	V

4. Switching characteristics are independent of operating junction temperature.

Normal Operation

Figure 1 illustrates a typical configuration. The external adapter provides power to the protection system so the circuitry is only active when the adapter is connected. The OVP monitors the voltage from the charger and if the voltage exceeds the overvoltage threshold, V_{th}, the OUT signal drives the gate of the MOSFET to within 1.0 V of V_{CC}, thus turning off the FET and disconnecting the source from the load. The nominal time it takes to drive the gate to this state is 400 nsec (1.0 μsec maximum for gate capacitance of < 12 nF). The CNTRL input can be used to interrupt charging and allow the microcontroller to measure the cell voltage under a normal condition to get a more accurate measure of the battery voltage. Once the overvoltage is removed, the MOSFET will be turned on again.

There are two events that will cause the OVP to turn off the MOSFET.

- Voltage on IN Rises Above the Overvoltage Detection Threshold
- CNTRL Input is Driven to a Logic HIGH

Adjusting the Overvoltage Detection Point with External Resistors

The separate IN and V_{CC} pins allow the user to adjust the overvoltage threshold, V_{th}, upwards by adding a resistor divider with the tap at the IN pin. However, the input impedance R_{in} does play a significant role in the calculation since it is several 10's of kΩ (R_{in} = 54 kΩ typical). The following equation shows the effects of R_{in}.

$$V_{CC} = V_x(1 + R_1/(R_2//R_{in})) \quad \text{(eq. 1)}$$

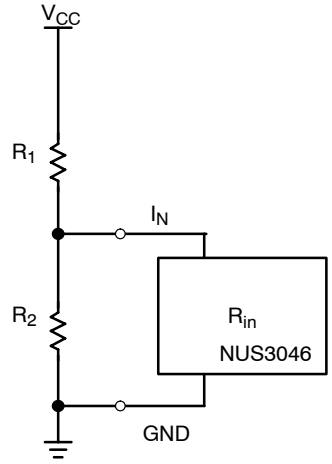


Figure 2. Voltage divider input to adjust overvoltage detection point

which equates to:

$$V_{CC} = V_x(1 + R_1/R_2 + R_1/R_{in}) \quad \text{(eq. 2)}$$

So, as R_{in} approaches infinity:

$$V_{CC} = V_x(1 + R_1/R_2) \quad \text{(eq. 3)}$$

This shows that R_{in} shifts the V_{th} detection point in accordance to the ratio of R_1 / R_{in}. However, if $R_1 << R_{in}$, this shift can be minimized. The following steps show this procedure.

Designing around the Maximum Voltage Rating Requirements, V(V_{CC}, IN)

The maximum breakdown voltage between pins V_{CC} and IN is 15 V. Therefore, care must be taken that the design does not exceed this voltage. Normally, the designer shorts V_{CC} to IN, V(V_{CC}, IN) is shorted to 0 V, so there is no issue. However, one must take care when adjusting the overvoltage threshold.

In Figure 2, the R1 resistor of the voltage divider divides the V(V_{CC}, IN) voltage to a given voltage threshold equal to:

$$(V_{CC}, IN) = V_{CC} * (R1/(R1 + (R2//R_{in}))) \quad \text{(eq. 4)}$$

V(V_{CC}, IN) worst case equals 15 V, and V_{CC} worst case equals 30 V, therefore, one must ensure that:

$$R1/(R1 + (R2//R_{in})) < 0.5 \quad \text{(eq. 5)}$$

Where 0.5 = V(V_{CC}, IN)max/V_{CCmax}

Therefore, the overvoltage threshold should be adjusted to voltage levels that are less than 15 V. If greater thresholds are desired, ON Semiconductor offers the NCP3045 which can withstand those voltages.

Design Steps for Adjusting the Overvoltage Threshold

1..Use Typical R_{in}, and V_{th} Values from the Electrical Specifications

2..Minimize R_{in} Effect by Selecting $R_1 << R_{in}$ since:

$$V_{OV} = V_{th}(1 + R_1/R_2 + R_1/R_{in}). \quad \text{(eq. 6)}$$

3..Let $X = R_{in} / R_1 = 100$.

4..Identify Required Nominal Overvoltage Threshold.

5..Calculate nominal R_1 and R_2 from Nominal Values:

$$R_1 = R_{in}/X \quad \text{(eq. 7)}$$

$$R_2 = \frac{R_1}{(V_{OV}/V_{th} - R_1/R_{in} - 1)} \quad \text{(eq. 8)}$$

6..Pick Standard Resistor Values as Close as Possible to these Values

7..Use min/max Data and Resistor Tolerances to Determine Overvoltage Detection Tolerance:

$$V_{OVmin} = V_{thmin}(1 + R_{1min}/R_{2max} + R_{1min}/R_{inmax}) \quad \text{(eq. 9)}$$

$$V_{OVtyp} = V_{thtyp}(1 + R_{1typ}/R_{2typ} + R_{1typ}/R_{intyp}) \quad \text{(eq. 10)}$$

$$V_{OVmax} = V_{thmax}(1 + R_{1min}R_{2max} + R_{1max}/R_{inmin}) \quad \text{(eq. 11)}$$

The specification takes into account the hysteresis of the comparator, so the minimum input threshold voltage (V_{th}) is the falling voltage detection point and the maximum is the rising voltage detection point. One should design the input supply such that its maximum supply voltage in normal operation is less than the minimum desired overvoltage threshold.

8..Use worst case resistor tolerances to determine the maximum $V(V_{CC},IN)$

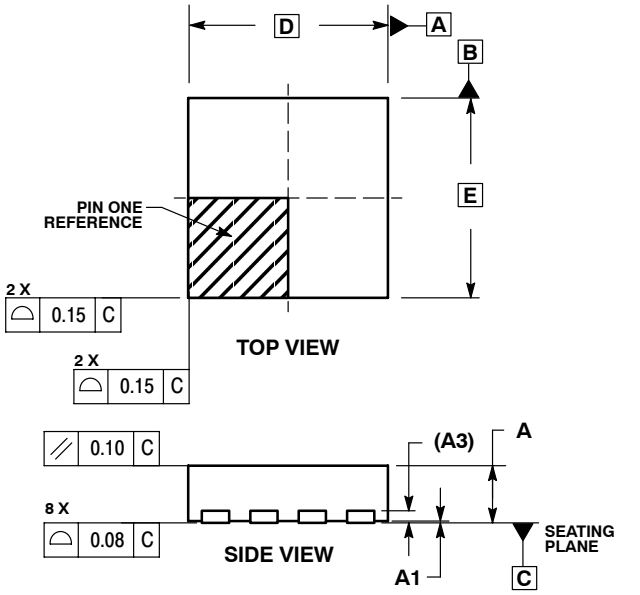
$$V(V_{CC}, IN)\,min = V_{CCmax} * (R1min/(R1min + R2max)) \quad \text{(eq. 12)}$$

$$V(V_{CC}, IN)typ = V_{CCmax} * (R1typ/(R1typ + R2typ)) \quad \text{(eq. 13)}$$

$$V(V_{CC}, IN)\,max = V_{CCmax} * (R1max/(R1max + R2min)) \quad \text{(eq. 14)}$$

PACKAGE DIMENSIONS

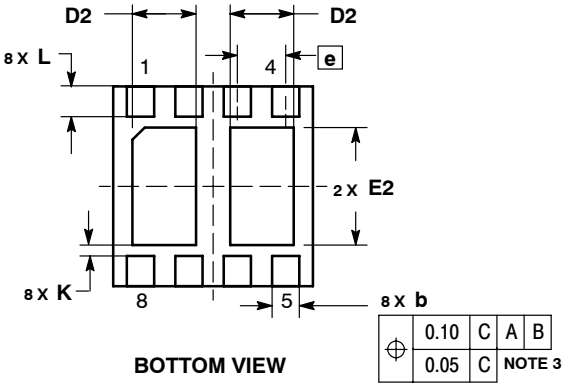
DFN8
CASE 506AL−01
ISSUE A



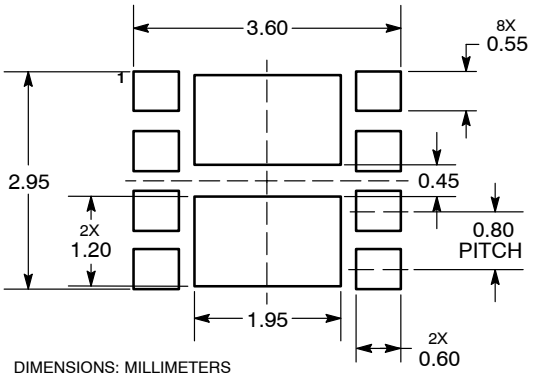
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3		0.20 REF	
b	0.35	0.40	0.45
D		3.30 BSC	
D2	0.95	1.05	1.15
E		3.30 BSC	
E2	1.80	1.90	2.00
e		0.80 BSC	
K	0.21	−−−	−−−
L	0.30	0.40	0.50

STYLE 1:
PIN 1. IN
2. GND
3. CNTRL
4. DRAIN
5. SOURCE
6. GATE
7. OUT
8. VCC



SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81−3−5773−3850

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative

NUS3046MN/D